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(54) Static random access type semiconductor memory device

Statische Direktzugriffsspeicheranordnung

Dispositif de mémoire semi-conductrice du type statique à accès aléatoire

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- INTERNATIONAL ELECTRON DEVICES MEETING December 1990, SAN FRANCISCO, CA, USA pages 477 - 480 , XP000279593 T. YAMANAKA ET AL. 'A 5.9um2 SUPER LOW POWER SRAM CELL USING A NEW PHASE-SHIFT LITHOGRAPHY'
- IEEE JOURNAL OF SOLID-STATE CIRCUITS vol. SC-20, no. 1, February 1985, NEW YORK, USA pages 178 - 201 S. D. S. MALHI ET AL. 'CHARACTERISTICS AND THREE-DIMENSIONAL INTEGRATION OF MOSFET'S IN SMALL-GRAIN LPCVD POLYCRYSTALLINE SILICON'

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Description

The present invention generally relates to semiconductor memory devices and, more particularly, relates to cell structures in a static random access memory where integration density of memory cells can be increased.

Fig. 7 is an equivalent circuit diagram of one memory cell in a conventional static random access memory (hereinafter referred to as SRAM). This memory cell includes thin-film p-type MOS transistors as loads. A pair of driver (for driving) transistors Q_1 and Q_2 (n-type MOS transistors) are connected to a pair of load transistors Q_5 and Q_6 (p-type MOS transistors) to form a flipflop circuit. The sources 110 and 111 of the pair of load transistors Q_5 and Q_6 are connected to a power supply Vcc and the sources 112 and 113 of driver transistors Q_1 and Q_2 are connected to GND. A pair of access transistors Q_3 and Q_4 (n-type MOS transistors) are connected to storage nodes 114 and 115, respectively. A bit line 107 is connected to one source/drain of access transistor Q_3 and a bit line 108 is connected to one source/drain of access transistor Q_4. The gates of access transistors Q_3 and Q_4 are connected to a word line 109.

Figs. 8 to 10 are plan views of the structure of an SRAM, showing three stages in order from the bottom on the surface of the substrate, respectively. Fig. 11 is a cross-sectional view of the structure taken along the line A-A in Figs. 8 to 10. Referring to Figs. 7, 8 to 11, a pair of driver transistors Q_1 and Q_2 and a pair of access transistors Q_3 and Q_4 are formed on a main surface of a p-type silicon substrate 148 of the memory cell. Driver transistor Q_1 includes a pair of source/drain regions 121 and 122 and a gate electrode 125. Driver transistor Q_2 includes a pair of source/drain regions 118 and 117 and a gate electrode 126. Access transistor Q_3 includes a pair of source/drain regions 119 and 120 and a gate electrode 109. Access transistor Q_4 includes a pair of source/drain regions 116 and 117 and a gate electrode 109. These transistors are n-type MOS transistors having source/drain regions formed on the main surface of p-type silicon substrate 148. Gate electrode 126 of driver transistor Q_2 is connected to source/drain region 120 of access transistor Q_3 through a contact 128. Gate electrode 126 of driver transistor Q_2 is connected to source/drain region 121 of driver transistor Q_1 through a contact 129. Gate electrode 125 of driver transistor Q_1 is connected to source/drain region 117 of access transistor Q_4 and source/drain region 117 of driver transistor Q_2 through a contact 127. A gate electrode 130 of a load transistor Q_5 is connected to a source/drain region 137 of a load transistor Q_6 through a contact 139. A gate electrode 131 of load transistor Q_6 is connected to a source/drain region 134 of load transistor Q_5 through a contact 138.

A bit line 107 is connected to source/drain region 119 of access transistor Q_3 through a contact 146 and a bit line 108 is connected to source/drain region 116 of access transistor Q_4 through a contact 147.

As stated above, in the memory cell of the conventional SRAM, four n-type MOS transistors are arranged on the silicon substrate and p-type thin film transistors are provided as loads above them. A case where a p-type thin film transistor is used as a load of a memory cell in an SRAM has been described in IEDM 1990 Technical Digest pp. 477-480. Fig. 13 is a cross-sectional view of a typical structure of a thin film transistor used as load transistors Q_5 and Q_6. The thin film transistor has a channel region 142 and a pair of source/drain regions 141 and 143 formed in a semiconductor layer such as polycrystalline silicon and a gate electrode 140 provided opposite to channel region 142 with an insulating layer interposed therebetween. Fig. 14 is a diagram showing a current characteristic of the thin film transistor.

In such an SRAM, it is necessary to reduce an area occupied by each memory cell in order to increase the integration density of the memory cells. However, the conventional memory cell above had two problems to be described below.

The first problem is that it is difficult to reduce an element isolation region between transistors making up the memory cell. Fig. 12 is a diagram showing by a model a cross-section of the structure of a LOCOS film 124 (Fig. 11) for insulating and isolating transistors from each other in the memory cell shown in Fig. 11. In this LOCOS film 152 (Fig. 12), regions X called "bird's beak" are formed at its both ends, which expand to the region where elements are formed, so that an isolation width W becomes larger than its desired value. For this reason, the width of the isolation region cannot be reduced, so that reduction in the size of the memory cell cannot be achieved.

The second problem concerns a current handling capability ratio β of a driver transistor to an access transistor (= the current handling capability of the driver transistor/the current handling capability of the access transistor). If the current handling capability ratio β is small, data is destroyed when it is read out from a memory cell. This phenomenon will now be described below. Figs. 15 (a) and (b) show two inverter circuits obtained by dividing the equivalent circuit of the memory cell shown in Fig. 7 in connection with the reading characteristic. In this case, load transistors Q_5 and Q_6 are not shown because the amount of the current flowing through these load transistors is little enough to be ignored compared with those of the access transistors and the driver transistors, so that is has no effect on the reading operation. The characteristic of reading from a memory cell is given from a change in voltage at one storage node obtained by fixing the bit line and the word line at Vcc and changing the gate voltage of the driver transistor (the voltage at the other storage node). Fig. 16(a) is a diagram showing the reading characteristic in a case where the current handling capability ratio β is large (about 3). The axis of abscissa represents a voltage at storage node 115 and

the axis of ordinate represents a voltage at storage node 114. The curve α_1 represents the voltage change characteristic at storage node 114 in a case where the voltage at storage node 115 is changed. The curve γ_1 shows the voltage change characteristic at storage node 115 in a case where the voltage at storage node 114 is changed. The curves α_1 and γ_1 intersect each other at three points P_1, P_2 and P_3. At point P_3, storage node 114 has "High" data stored, and storage node 115 has "High" data stored at point P_1. Point P_2 is an unstable point and the condition at this point P_2 is not kept at the time of reading. In the figure, a region surrounded by a circle h is called "eye of a memory cell". As the current handling capability ratio β of the transistors is larger, the circle h becomes bigger and the reading operation is stabilized.

In order to reduce the size of a memory cell, the size of an access transistor or a driver transistor is reduced. The access transistor or the driver transistor is reduced in size, for example, by shortening the gate length. If the transistor width of the access transistor is reduced to 1μm or less, a so-called narrow channel effect becomes significant, so that a threshold voltage Vth of the access transistor is increased. Fig. 16(b) shows the voltage change characteristic at the storage node in a case where the threshold voltage Vth of the access transistor is increased. In Figs. 16(a) and (b), Vcc-θ or Vcc-θ' corresponds to the threshold voltage Vth of the access transistor. As shown in Fig. 16(b), if the threshold voltage of the access transistor is increased, the curves α_2 and γ_2 intersect each other at one point P_2 only and the so-called "eye of a memory cell" region disappears. As a result, the stable points of the voltage at each storage node disappear, and data stored in the memory cell is destroyed at the time of the reading operation. For these reasons, the access transistor cannot be reduced in size even though the size of the driver transistor can be reduced. If only the driver transistor is reduced in size, the current handling capability ratio β of the both transistors becomes small, making the reading operation unstable.

IEEE J. Solid-State Circuits, Vol. SG-20, No.1, Feb. 1985, pp. 178 - 201, (Mahli et al.) discloses different types of thin film transistors in SOI technique and their characteristics.

An object of the present invention is to reduce the size of a memory cell and stabilize the operation of reading out stored data in an SRAM.

This object is achieved by a semiconductor memory device according to claim 1.

Further developments of the invention are given in the subclaims.

The semiconductor memory device includes a memory cell including a pair of driver transistors of a first conductivity type and a pair of load transistors of a second conductivity type making up a flipflop circuit, and a pair of access transistors, all transistors being thin film transistors. The semiconductor memory device further includes a semiconductor substrate having a main surface, an insulating layer formed on the semiconductor substrate, a first group of said thin film transistors arranged on the insulating layer, an interlayer insulating layer covering the surface of the first group of thin film transistors and a second group of said thin film transistors arranged on the interlayer insulating layer. The first group of thin film transistors includes at least one transistor of the driver transistors, the load transistors and the access transistors. The second group of thin film transistors includes at least one transistor of the driver transistor, the load transistor and the access transistor excluding the transistor included in the first group of thin film transistors.

The six transistors making up a memory cell are thin film transistors. Element isolation is made by providing the interlayer insulating layer between the thin film transistors. Accordingly, an area of an element isolation region can be reduced by eliminating the conventional element isolation structure using a LOCOS film.

Therefore, a narrow channel effect can be restrained and stabilization of the operation of reading out stored data as well as reduction in size of a memory cell can be achieved by forming a thin film transistor as an access transistor.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying figures.

Fig. 1 is a plan view of the structure of a memory cell in an SRAM according to an embodiment of the present invention.

Fig. 2 is a plan view showing the structure of an upper layer portion of the memory cell shown in Fig. 1.

Fig. 3 is a cross-sectional view showing a typical structure of a thin film transistor used in this invention.

Fig. 4 is a diagram showing an electrical characteristic of the thin film transistor shown in Fig. 3.

Fig. 5 is a structural cross-sectional view taken along the line B-B shown in Figs. 1 and 2.

Fig. 6 is a structural cross-sectional view taken along the line C-C in Figs. 1 and 2.

Fig. 7 is an equivalent circuit diagram of a memory cell in a conventional SRAM.

Fig. 8 is a structural plan view of a memory cell in a conventional SRAM.

Fig. 9 is a structural plan view of a still upper layer of the memory cell shown in Fig. 8.

Fig. 10 is a structural plan view of a still upper layer of the memory cell shown in Fig. 9.

Fig. 11 is a structural cross-sectional view taken along the line A-A in Figs. 8 to 10.

Fig. 12 is a cross-sectional view of the structure in the vicinity of a LOCOS film used in isolating elements in a conventional memory cell.

Fig. 13 is a cross-sectional view showing the structure of a typical cross section of a thin film transistor used as a conventional load transistor.

Fig. 14 is a diagram showing an electrical characteristic of the thin film transistor shown in Fig. 45.

Fig. 15 is an equivalent circuit diagram (a), (b) showing two inverter circuits obtained by dividing the flipflop circuit shown in Fig. 7.

Fig. 16 is a diagram (a), (b) showing the characteristic curve of reading out data of a conventional memory cell.

A memory cell according to an embodiment includes pairs of access transistors Q_3 and Q_4, driver transistors Q_1 and Q_2 and load transistors Q_5 and Q_6 which are all thin film transistors. An equivalent circuit of this memory cell is equal to that shown in Fig. 7.

The structure of the memory cell will now be described with reference to Fig. 7 and further to Figs. 1, 2, 5 and 6. A main surface of a silicon substrate 32 has an insulating layer 33a formed thereon. A pair of access transistors Q_3 and Q_4 and a pair of driver transistors Q_1 and Q_2 are arranged on the surface of insulating layer 33a. The four transistors Q_1 to Q_4 are n-type thin film transistors. Access transistor Q_3 includes a pair of source/drain regions 1 and 3 and a channel region 2 formed in a polycrystalline silicon layer and a gate electrode 10. Access transistor Q_4 includes a pair of source/drain regions 6 and 8 and a channel region 7 formed in a polycrystalline silicon layer and a gate electrode 10. Driver transistor Q_1 includes a pair of source/drain regions 3 and 5 and channel region 4 formed in the polycrystalline silicon layer and a gate electrode 11. Driver transistor Q_2 includes a pair of source/drain regions 8 and 5 and a channel region 9 formed in the polycrystalline silicon layer and a gate electrode 12. The surfaces of these four transistors Q_1 to Q_4 are covered with a first interlayer insulating layer 33b.

A pair of p-type load transistors Q_5 and Q_6 are formed on the surface of first interlayer insulating layer 33b. Load transistor Q_5 includes a pair of source/drain regions 13 and 15, a channel region 14 and a gate electrode 11. Load transistor Q_5 shares gate electrode 11 with driver transistor Q_1. Load transistor Q_6 includes a pair of source/drain regions 13 and 17, a channel region 16 and a gate electrode 12. Load transistor Q_6 shares gate electrode 12 with driver transistor Q_2. The surfaces of load transistors Q_5 and Q_6 are covered with a second interlayer insulating layer 33c.

A pair of bit lines 107 and 108 are formed on the surface of second interlayer insulating layer 13c. Bit line 107 is connected to source/drain region 1 of access transistor Q_3 through a contact 26. Bit line 108 is connected to source/drain region 6 of access transistor Q_4 through a contact 27. Source/drain region 15 of load transistor Q_5 is connected to source/drain region 3 shared by access transistor Q_3 and driver transistor Q_1 through a contact 20. A contact 23 connects source/drain region 15 of load transistor Q_5 to an interconnection layer 18. A contact 22 connects interconnection layer 18 to gate electrode 12 of load transistor Q_6. A contact 21 connects source/drain region 17 of load transistor Q_6 to gate electrode 11 of load transistor Q_5. A contact 19 connects gate electrode 11 of load transistor Q_5 to source/drain region 8 of driver transistor Q_2.

Fig. 3 is a diagram showing by a model the structure of a typical cross section of a thin film transistor used in the embodiment. Fig. 4 shows an electrical characteristic of the thin film transistor shown in Fig. 3.

As stated above, since all the six transistors in the memory cell are thin film transistors, it is possible to prevent an increase in the threshold voltage of the access transistor under the influence of the narrow channel effect. Accordingly, the sizes of the access transistor and the driver transistor can be determined so that the current handling capability ratio β of the driver transistor to the access transistor is large. As a result, a memory cell can be constructed in which a stable reading operation can be performed.

As stated above, in accordance with one aspect of the present invention, all the transistors making up the memory cell are thin film transistors and the transistors are insulated and isolated from each other without using a LOCOS film, so that miniaturization of the cell structure by reduction in the size of the isolation region can be realized.

Claims

1. A semiconductor memory device including a memory cell constituted by a pair of thin film driver transistors (Q_1, Q_2) of a first conductivity type and a pair of thin film load transistors (Q_5, Q_6) of a second conductivity type making up a flipflop circuit, and a pair of thin film access transistors (Q_3, Q_4), comprising:

   a semiconductor substrate (32) having a main surface;
   an insulating layer (33a) formed on said main surface of the semiconductor substrate;
   a first group consisting of at least one of said thin film transistors (1 to 12) and arranged on said insulating layer (33a).
   an interlayer insulating layer (33b) covering the surface of said first group of thin film transistors (1-12); and
   a second group consisting of the remainder of said thin film transistors (11 to 17) of said memory cell and arranged on said interlayer insulating layer (33b).

2. The semiconductor memory device according to claim 1, wherein said first group of thin film transistors includes said driver transistors (Q_1, Q_2) and said access transistors (Q_3, Q_4) and said second group of thin film transistors includes said load transistors (Q_5, Q_6).

3. The semiconductor memory device according to

claims 1 or 2, wherein each transistor in said first group of thin film transistors includes a pair of impurity regions (1, 3, 5, 6, 8) formed in a first semiconductor layer on said insulating layer (33a) and each transistor in said second group of thin film transistors includes a pair of impurity regions (13, 15, 17) formed in a second semiconductor layer on said interlayer insulating layer (33b).

4. The semiconductor memory device according to claim 3, wherein a gate electrode of said driver transistor (Q_1, Q_2) included in said first group of thin film transistors and gate electrode of said load transistor (Q_5, Q_6) included in said second group of thin film transistors are formed of a common layer (11, 12), and

said first semiconductor layer included in said first group of thin film transistors and said second semiconductor layer included in said second group of thin film transistors are arranged opposing each other with said common layer (11,12) interposed therebetween.

Patentansprüche

1. Halbleiterspeichervorrichtung, die eine Speicherzelle aufweist, die durch ein Paar von Dünnschicht-Treibertransistoren (Q_1, Q_2) eines ersten Leitungstyps und ein Paar von Dünnschicht-Lasttransistoren (Q_5, Q_6) eines zweiten Leitungstyps, die eine Flip-Flop-Schaltung bilden, und ein Paar von Dünnschicht-Zugriffstransistoren (Q_3, Q_4) gebildet wird, die aufweist:

ein Halbleitersubstrat (32), das eine Hauptoberfläche aufweist, eine Isolierschicht (33a), die auf der Hauptoberfläche des Halbleitersubstrates ausgebildet ist,
eine erste Gruppe, die aus mindestens einem der Dünnschicht-Transistoren (1 bis 12) besteht und auf der Isolierschicht (33a) angeordnet ist,
eine Zwischenschicht-Isolierschicht (33b), die die Oberfläche der ersten Gruppe von Dünnschicht-Transistoren (1 bis 12) bedeckt, und
eine zweite Gruppe, die aus dem Rest der Dünnschicht-Transistoren der Speicherzelle besteht und auf der Zwischenschicht-Isolierschicht (33b) angeordnet ist.

2. Halbleiterspeichervorrichtung nach Anspruch 1, bei der die erste Gruppe der Dünnschicht-Transistoren die Treibertransistoren (Q_1, Q_2) und die Zugriffstransistoren (Q_3, Q_4) enthält und die zweite Gruppe der Dünnschicht-Transistoren die Lasttransistoren (Q_5, Q_6) enthält.

3. Halbleiterspeichervorrichtung nach Anspruch 1 oder 2, bei der jeder Transistor in der ersten Gruppe der Dünnschicht-Transistoren ein Paar von Dotierungsbereichen (1, 3, 5, 6, 8), die in einer ersten Halbleiterschicht auf der Isolierschicht (33a) ausgebildet sind, enthält, und jeder Transistor in der zweiten Gruppe der Dünnschicht-Transistoren ein Paar von Dotierungsbereichen (13, 15, 17), die in einer zweiten Halbleiterschicht auf der Zwischenschicht-Isolierschicht (33b) ausgebildet sind, enthält.

4. Halbleiterspeichervorrichtung nach Anspruch 3, bei der eine Gateelektrode des Treibertransistors (Q_1, Q_2), der in der ersten Gruppe von Dünnschicht-Transistoren enthalten ist, und eine Gateelektrode des Lasttransistors (Q_5, Q_6), der in der zweiten Gruppe von Dünnschicht-Transistoren enthalten ist, aus einer gemeinsamen Schicht (11, 12) ausgebildet sind, und die erste Halbleiterschicht, die in der ersten Gruppe von Dünnschicht-Transistoren enthalten ist, und die zweite Halbleiterschicht, die in der zweiten Gruppe von Dünnschicht-Transitoren enthalten ist, einander gegenüberliegend angeordnet sind, wobei die gemeinsame Schicht (11, 12) dazwischengesetzt ist.

Revendications

1. Un dispositif de mémoire à semiconducteurs comprenant une cellule de mémoire constituée par une paire de transistors d'attaque à couches minces (Q_1, Q_2) d'un premier type de conductivité, et une paire de transistors de charge à couches minces (Q_5, Q_6), d'un second type de conductivité, constituant un circuit de bascule, et par une paire de transistors d'accès à couches minces (Q_3, Q_4), comprenant :

un substrat semiconducteur (32) ayant une surface principale;
une couche isolante (33a) formée sur la surface principale du substrat semiconducteur;
un premier groupe constitué par l'un au moins des transistors à couches minces précités (1 à 12) et disposé sur la couche isolante (33a);
une couche d'isolation inter-couche (33b) recouvrant la surface du premier groupe de transistors à couches minces (1-12); et
un second groupe constitué par le reste des transistors à couches minces précités (11 à 17) de la cellule de mémoire, et disposé sur la couche d'isolation inter-couche (33b).

2. Le dispositif de mémoire à semiconducteurs selon la revendication 1, dans lequel le premier groupe de transistors à couches minces comprend les tran-

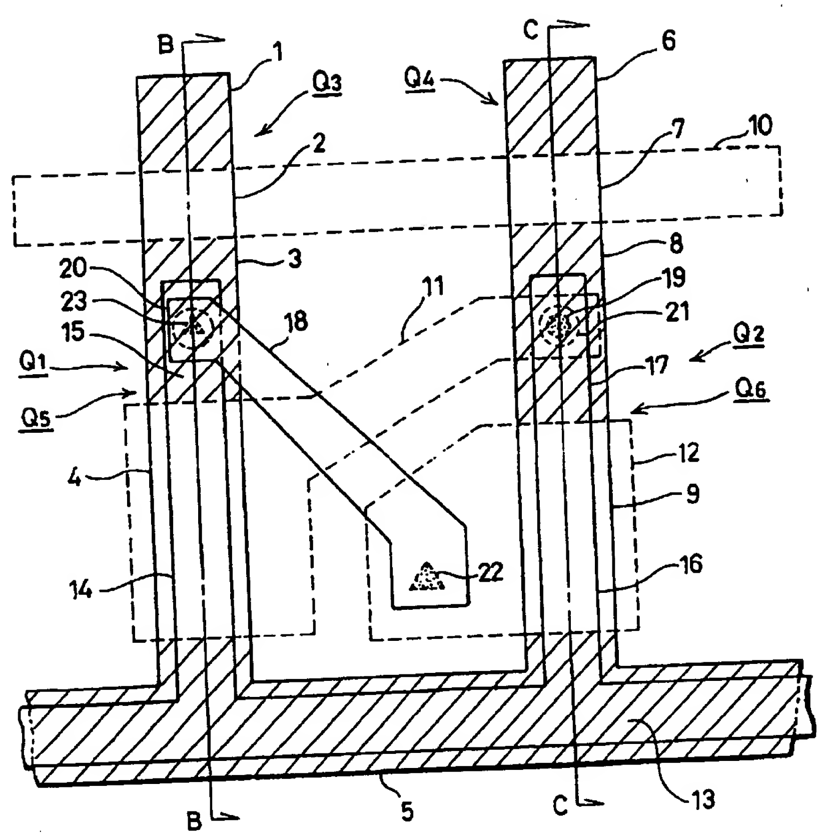
sistors d'attaque (Q_1, Q_2) et les transistors d'accès (Q_3, Q_4) et le second groupe de transistors à couches minces comprend les transistors de charge (Q_5, Q_6).

3. Le dispositif de mémoire à semiconducteurs selon les revendications 1 ou 2, dans lequel chaque transistor du premier groupe de transistors à couches minces comprend une paire de régions d'impuretés (1, 3, 5, 6, 8) formées dans une première couche de semiconducteur sur la couche isolante (33a), et chaque transistor dans le second groupe de transistors à couches minces comprend une paire de régions d'impuretés (13, 15, 17) formées dans une seconde couche de semiconducteur sur la couche d'isolation inter-couche (33b).

4. Le dispositif de mémoire à semiconducteurs selon la revendication 3, dans lequel une électrode de grille du transistor d'attaque (Q_1, Q_2) qui fait partie du premier groupe de transistors à couches minces et une électrode de grille du transistor de charge (Q_5, Q_6) qui fait partie du second groupe de transistors à couches minces sont formées par une couche commune (11, 12), et

la première couche de semiconducteur qui est incluse dans le premier groupe de transistors à couches minces et la seconde couche de semiconducteur qui est incluse dans le second groupe de transistors à couches minces sont disposées face à face avec la couche commune (11, 12) interposée entre elles.

FIG.1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1
Q3
Q4
C
6
2
7
10
20
3
8
23
19
15
18
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17
Q5
Q6
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13
B
5
C

FIG. 2

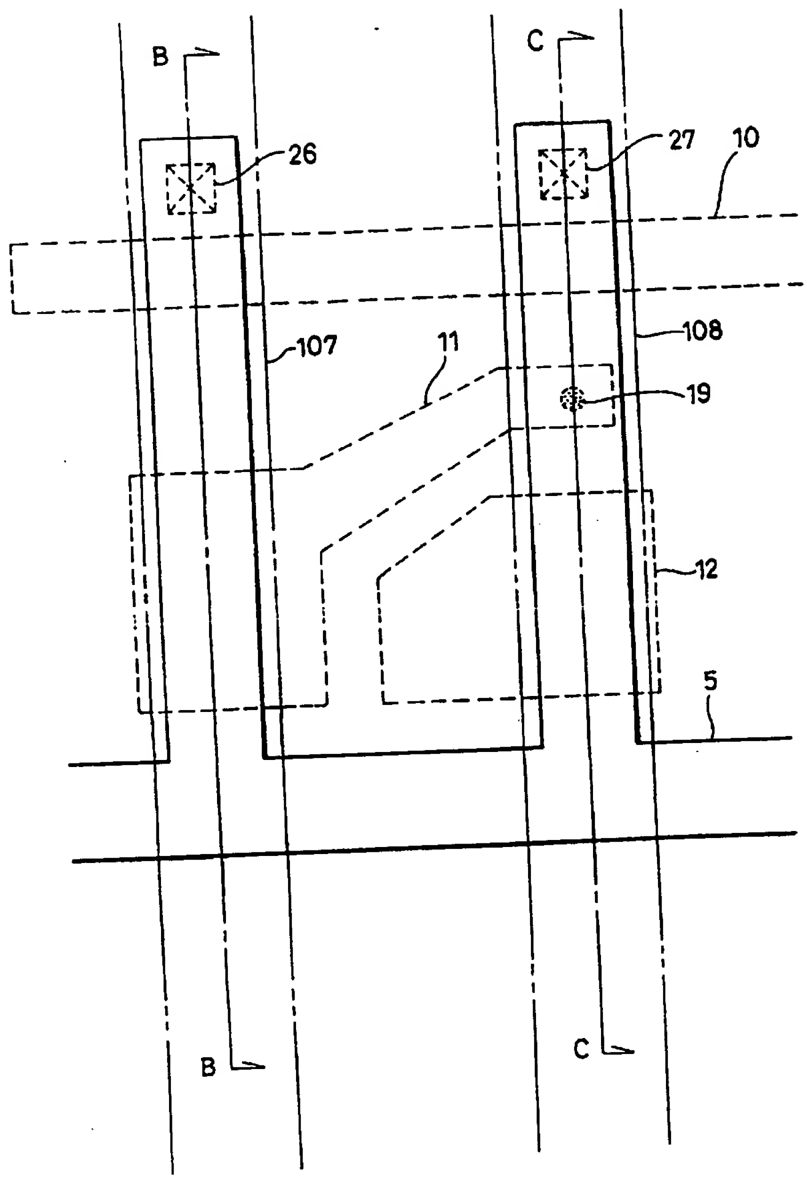


FIG. 3

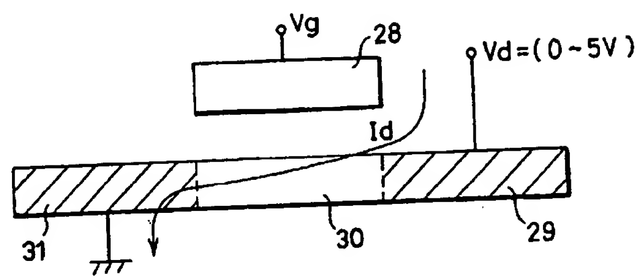


FIG.4

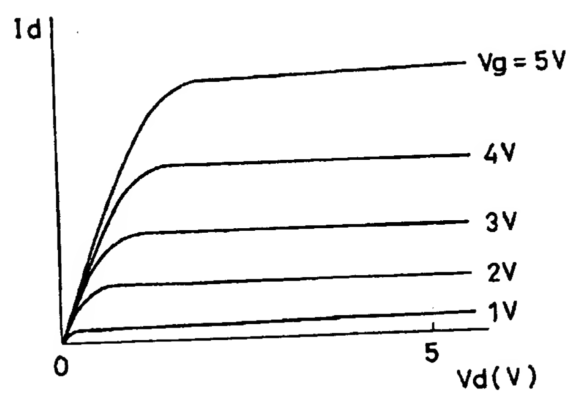


FIG.5

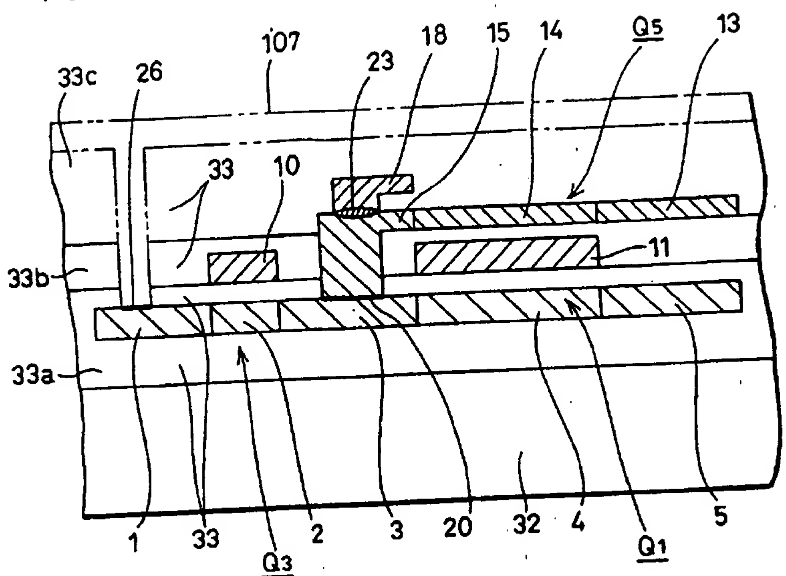
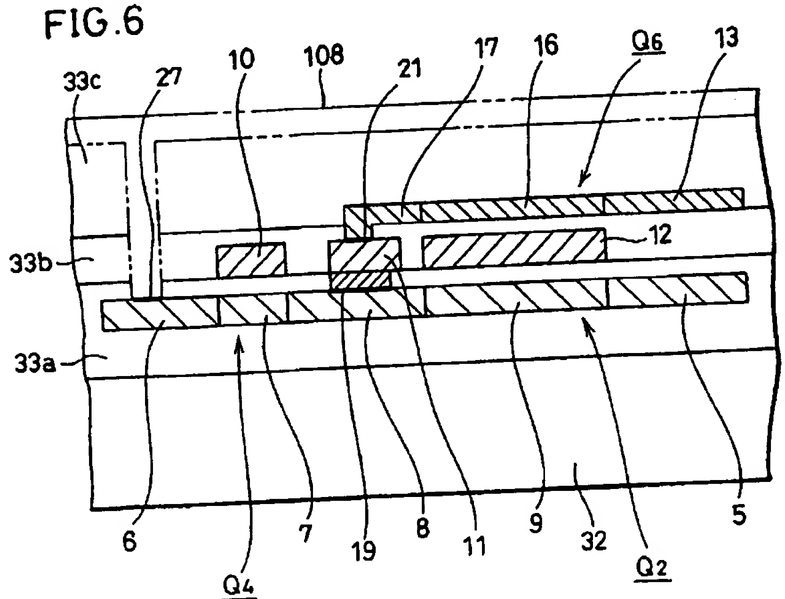

107
33c
26
23
18
15
14
Q5
13
33
10
11
33b
33a
1
33
Q3
2
3
20
32
4
Q1
5

FIG.6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27
10
108
21
17
16
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Q4
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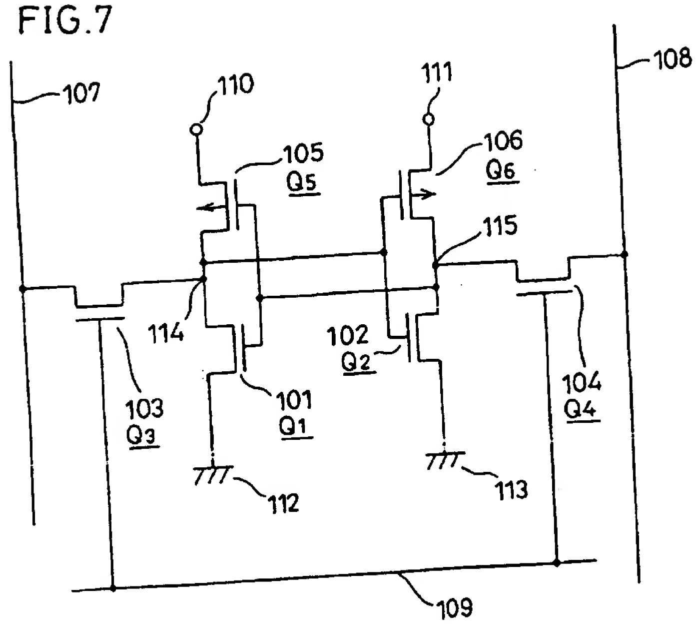
32
Q2
5

FIG.7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110
111
108
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Q5
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Q6
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Q2
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Q1
103
Q3
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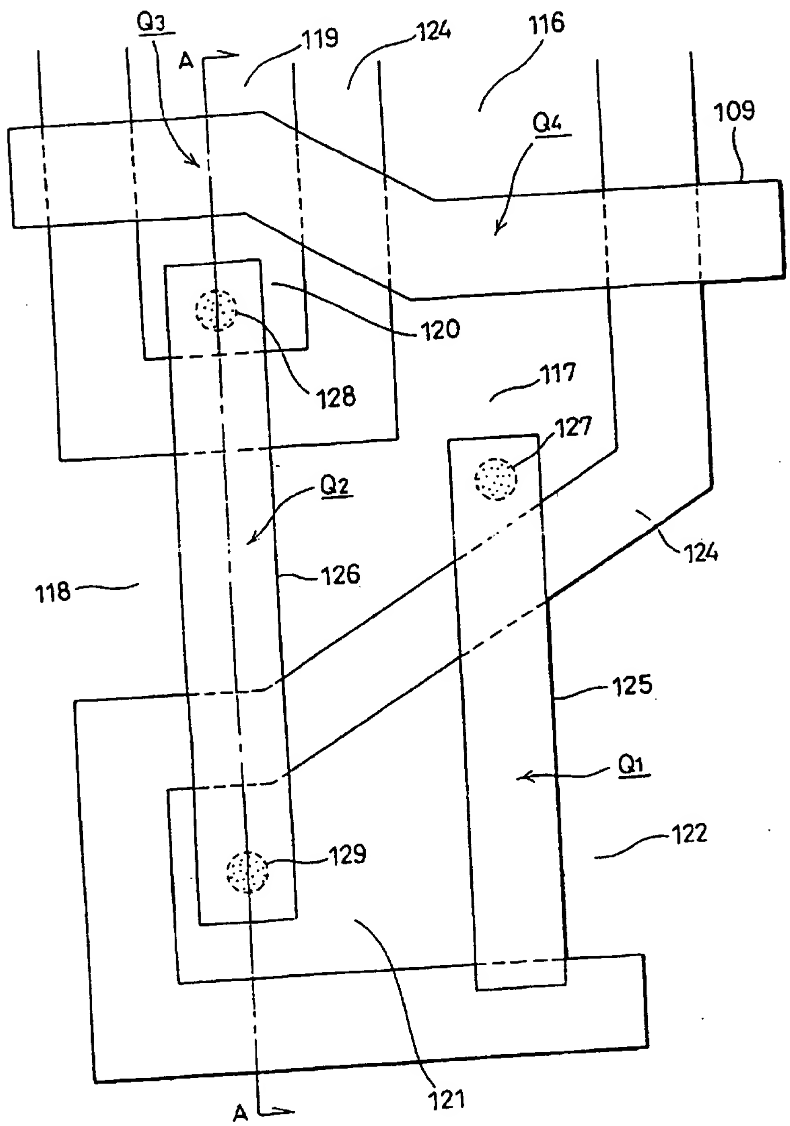
Q4
112
113
109

FIG. 8


Q3
A
119
124
116
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Q4
120
128
117
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Q2
124
118
126
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Q1
122
129
121
A

FIG.9

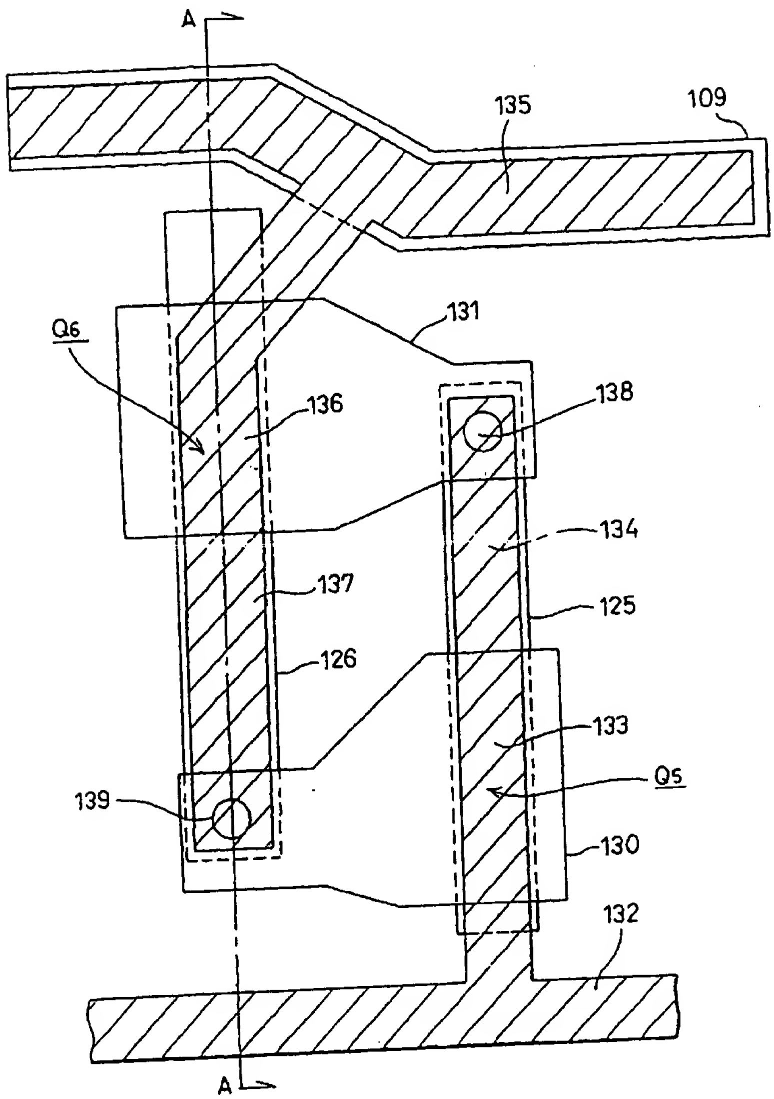


FIG.10

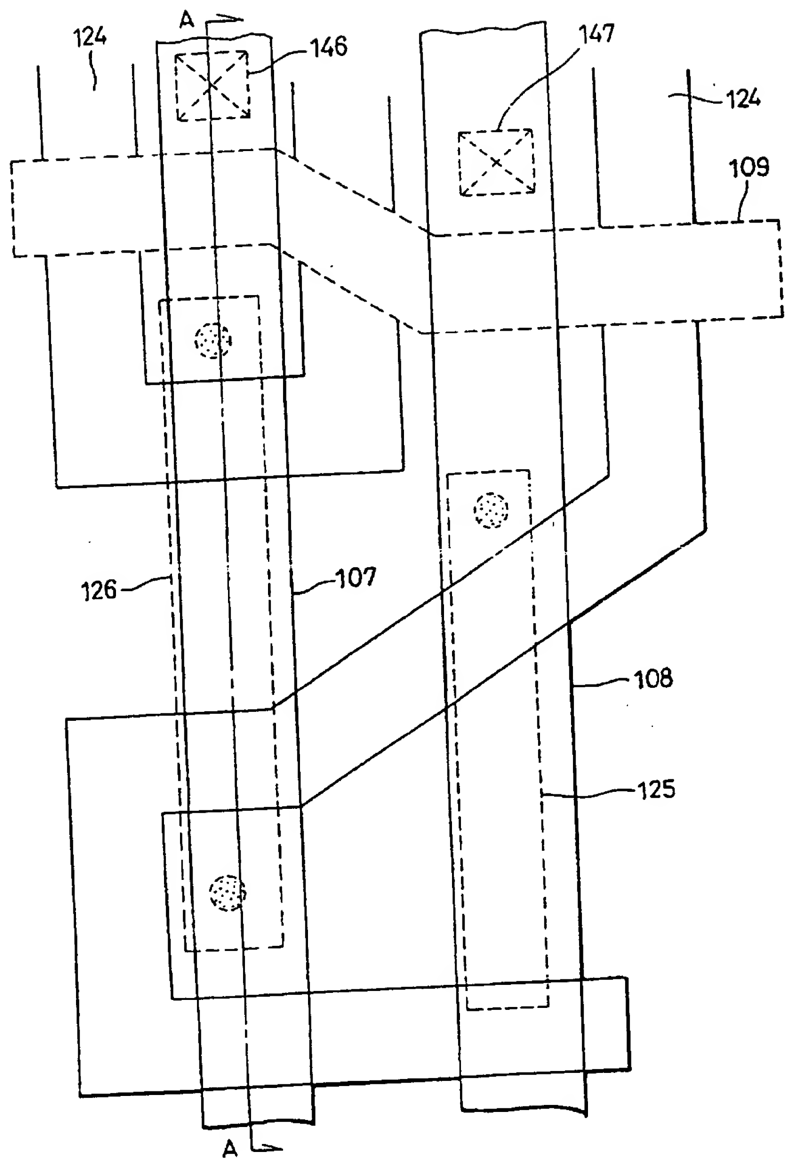
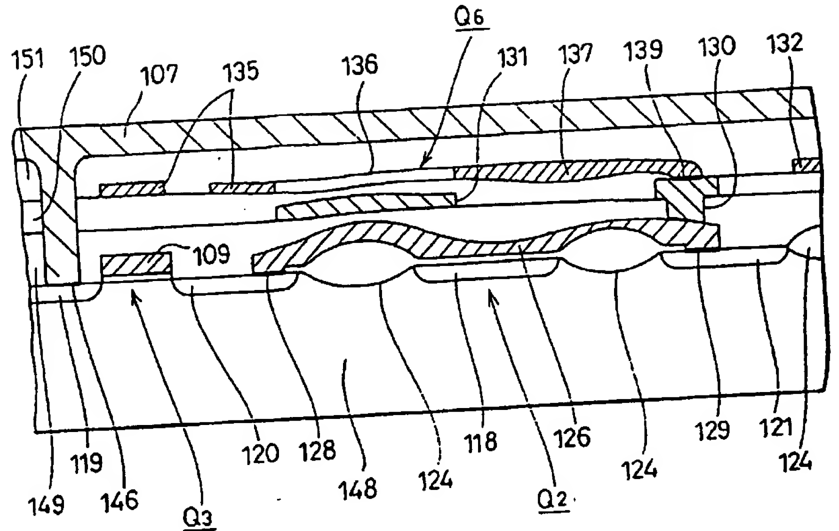


FIG.11


Q6
151
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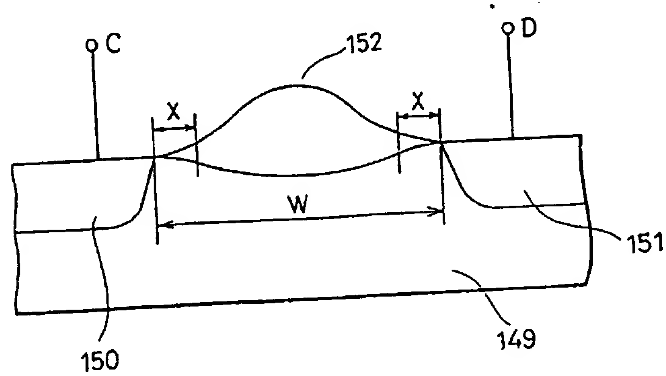
124

FIG.12


C
D
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X
X
W
151
150
149

FIG.13

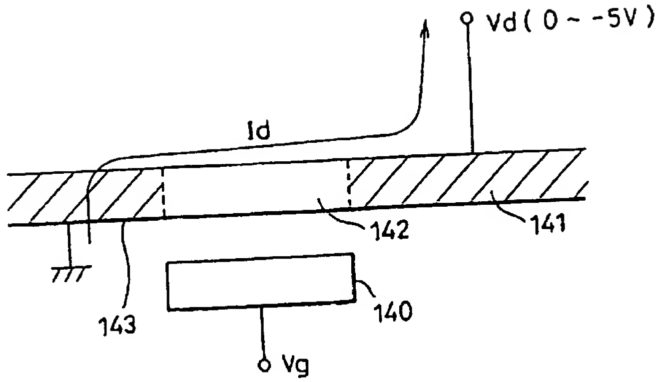


FIG.14

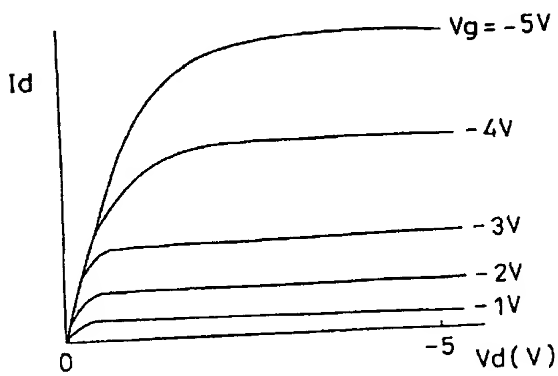
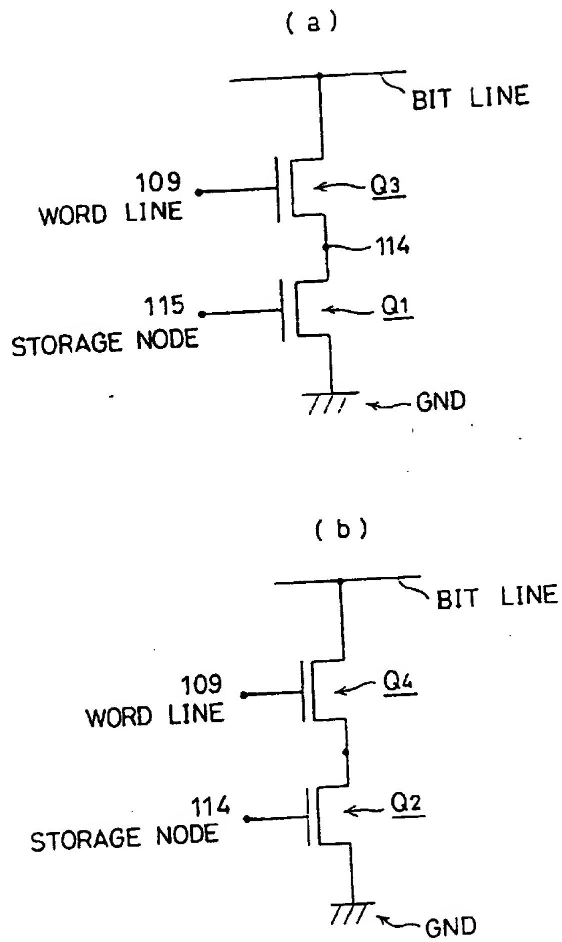


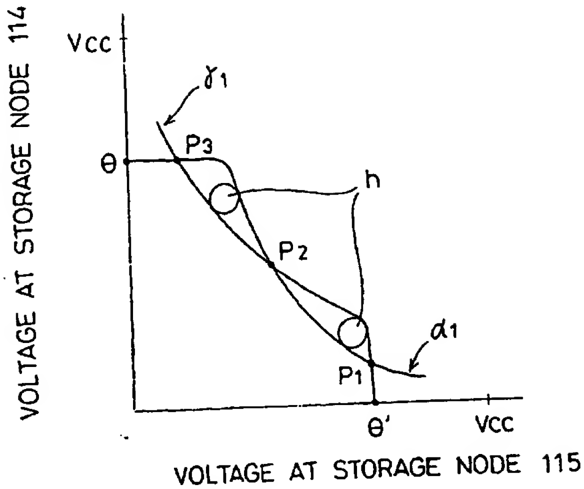
FIG.15



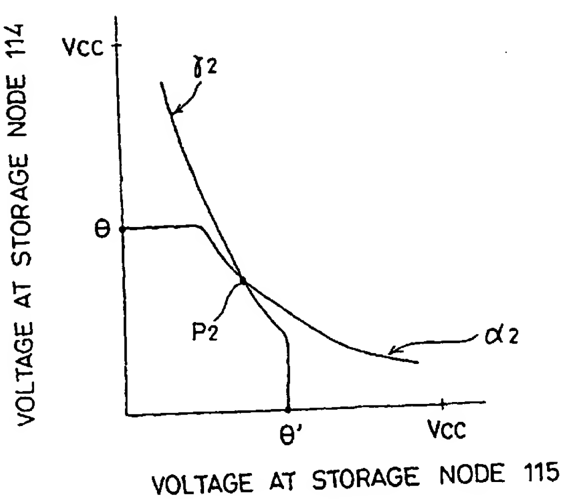
(a)
BIT LINE
109
WORD LINE
Q3
114
115
STORAGE NODE
Q1
GND
(b)
BIT LINE
109
WORD LINE
Q4
114
STORAGE NODE
Q2
GND

FIG.16

(a)


VOLTAGE AT STORAGE NODE 114
Vcc
γ1
P3
θ
h
P2
α1
P1
θ'
Vcc
VOLTAGE AT STORAGE NODE 115

(b)


VOLTAGE AT STORAGE NODE 114
Vcc
γ2
θ
P2
α2
θ'
Vcc
VOLTAGE AT STORAGE NODE 115